REMARKS

The Examiner is thanked for the thorough examination and search of the subject patent application and for finding patentable material in the claims.

Claims 11-13, 15, 17, 19, 20, 23-25, 42-56, 58, 60-69, 71, 73, 74, 102-107, 109-111, 117-121, 123-129, 132-141, 143-149, 151-154, 156, 158-163, 165-169, 171-175, 177-186, 188, 195-200, 202, 209-211 and 213-234 are pending; Claims 11-13, 15, 17, 19, 20, 24, 25, 42-48, 50-53, 55, 56, 60, 61, 63-69, 73, 74, 102, 104, 105, 107, 109, 110, 117-120, 123, 124, 126-129, 132-141, 144-149, 151-154, 158-160, 162, 163, 165-167, 171-173, 175, 177-179, 181-183, 185, 186, 188, 195, 197-200, 209, 214, 215, 220-222, 227-229 and 234 have been currently amended; Claims 1-10, 14, 16, 18, 21, 22, 26-41, 57, 59, 70, 72, 75-101, 108, 112-116, 122, 130, 131, 142, 150, 155, 157, 164, 170, 176, 187, 189-194, 201, 203-208 and 212 have been canceled.

Response to Claim Rejection under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 42-51, 151-154 and 214-220

As currently amended, independent Claim 42 is recited below:

42. A method of fabricating a chip package comprising the steps of:

providing a first die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads;

depositing an adhesive material on a substrate;

joining a first side of said first die and said substrate using said adhesive material, wherein a first opening in said substrate exposes said first side of said first die, wherein said first opening in said substrate is over one of said multiple pads, and wherein said passivation layer at said first side;

joining a first side of a second die and said substrate using said adhesive material, wherein a second opening in said substrate exposes said first side of said second die;

encapsulating a second side and sidewall of said first die, a second side and sidewall of said second die, and a gap between said first and second dies with a molding material, wherein said second side of said first die is opposite to said first side of said first die, and said second side of said second die is opposite to said first side of said second die, wherein said gap is filled completely with said molding material, and wherein said molding material has a surface with a first region over said gap and multiple second regions over said second side of said first die and over said second side of said second die, wherein said first region is at a same horizontal level as said multiple second regions; and

after said encapsulating said second side and sidewall of said first die, said second side and sidewall of said second die, and said gap between said first and second dies with said molding material, separating said molding material and said substrate into multiple portions to form said chip package, wherein said separating said molding material and said substrate comprises a sawing process.

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Reconsiderations of Claims 42, 48, 50 and 214-219 rejected under 35 U.S.C. 102(e) as being anticipated by Fillion et al. (U.S. Pat. No. 6,306,680) and of Claims 46, 47, 49, 51, 151, 152, 214 and 220 rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion et al. are requested in accordance with the following remarks.

Applicants respectfully assert that the method currently claimed in Claim 42 patentably distinguishes over the citation by Fillion et al. (U.S. Pat. No. 6,306,680).

The Examiner considers that Fillion et al. teach the subject matter of encapsulating a top side of a die with a molding material. ~ *See lines 10-12 on page 3, in the last Office Action mailed Oct. 5, 2007* ~

Applicants respectfully traverse the Examiner's opinion because Fillion et al. fail to teach, hint or suggest that a top side of a die 102 can be encapsulated by a molding material 130, but teach only sidewalls of the die 102 can be encapsulated by the molding material 130. ~ *See Fig. 4* ~

It is believed that Fillion et al. fail to teach, hint or suggest that a second side of a die, opposite to a first side, joined with a substrate, of the die may be encapsulated with a molding material, as shown in Fig. 2g and as currently claimed in Claim 42.

Furthermore, Fillion et al. fail to teach, hint or suggest that a die, separated from a wafer, may comprise a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, as taught on pages 9-10 of the Specification and as currently claimed in Claim 42.

Withdrawal of rejection under 35 U.S.C. 102(e) to currently-amended Claim 42 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 42 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 43-51, 151-154 and 214-220 patently define over the prior art as well.

Response to Claims 63-69, 71, 73, 74, 162, 163 and 165-168

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As currently amended, independent Claim 63 is recited below:

63. A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said overlying metal layer is on said multiple pads;

joining said die and a substrate, wherein an opening in said substrate exposes said overlying metal layer of said die;

after said joining said die and said substrate, forming a metal conductor through said opening in said substrate; and

after said joining said die and said substrate, separating said substrate into multiple portions.

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Reconsiderations of Claims 63, 66, 71, 73 and 74 rejected under 35 U.S.C. 102(e) as being anticipated by Fillion et al. (U.S. Pat. No. 6,306,680) and of Claims 64, 65 and 165-168 rejected

under 35 U.S.C. 103(a) as being unpatentable over Fillion et al. are requested in accordance with the following remarks.

Applicants respectfully assert that the method currently claimed in Claim 63 patentably distinguishes over the citation by Fillion et al. (U.S. Pat. No. 6,306,680) because Fillion et al. fail to teach, hint or suggest an opening in a substrate joined with a die may expose an overlying metal layer on multiple pads exposed by multiple openings in a passivation layer, as currently claimed in Claim 63.

Furthermore, Fillion et al. fail to teach, hint or suggest that a die, separated from a wafer, may comprise a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said overlying metal layer is on said multiple pads, as taught on pages 9-10 of the Specification and as currently claimed in Claim 63.

Withdrawal of rejection under 35 U.S.C. 102(e) to currently-amended Claim 63 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 63 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 64-69, 71, 73, 74, 162, 163 and 165-168 patently define over the prior art as well.

Response to Claims 134-141, 143-145, 185, 186, 188 and 228-234

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As currently amended, independent Claim 134 is recited below:

134. A method of fabricating a chip package comprising the steps of:

separating a wafer into multiple dies, wherein one of said multiple dies comprises a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads;

after said separating said wafer, joining a first side of said one of said multiple dies and a substrate, wherein an opening in said substrate exposes said first side of said one of said multiple dies, wherein said passivation layer is at said first side;

after said joining said first side of said one of said multiple dies and said substrate, forming a metal conductor through said opening in said substrate;

after said joining said first side of said one of said multiple dies and said substrate, encapsulating a second side and sidewall of said one of said multiple dies with a molding material, wherein said first side of said one of said multiple dies is opposite to said second side of said one of said multiple dies; and

after said encapsulating said second side and sidewall of said one of said multiple dies with said molding material, separating said molding material and said substrate into multiple portions to form said chip package, wherein said separating said molding material and said substrate comprises a sawing process.

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Reconsiderations of Claims 134, 136, 139 and 229-233 rejected under 35 U.S.C. 102(e) as being anticipated by Fillion et al. (U.S. Pat. No. 6,306,680) and of Claims 140, 141, 144, 145, 188, 228 and 234 rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion et al. are requested in accordance with the following remarks.

Applicants respectfully assert that the method currently claimed in Claim 134 patentably distinguishes over the citation by Fillion et al. (U.S. Pat. No. 6,306,680).

The Examiner considers that Fillion et al. teach the subject matter of encapsulating a top side of a die with a molding material. ~ *See lines 8 and 9 on page 5, in the last Office Action mailed Oct. 5, 2007* ~

Applicants respectfully traverse the Examiner's opinion because Fillion et al. fail to teach, hint or suggest that a top side of a die 102 can be encapsulated by a molding material 130, but teach only sidewalls of the die 102 can be encapsulated by the molding material 130. ~ *See Fig. 15* ~

It is believed that Fillion et al. fail to teach, hint or suggest that a second side of a die, opposite to a first side, joined with a substrate, of the die may be encapsulated with a molding material, as shown in Fig. 2g and as currently claimed in Claim 134.

Furthermore, Fillion et al. fail to teach, hint or suggest that a die, separated from a wafer, may comprise a semiconductor substrate, multiple integrated circuit devices on said

semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, as taught on pages 9-10 of the Specification and as currently claimed in Claim 134.

Withdrawal of rejection under 35 U.S.C. 102(e) to currently-amended Claim 134 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 134 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 135-141, 143-145, 185, 186, 188 and 228-234 patently define over the prior art as well.

Response to Claims 197-200 and 202

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As currently amended, independent Claim 197 is recited below:

197. A method of fabricating a chip package comprising the steps of:
providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, wherein said

overlying metal layer is on said multiple pads exposed by said multiple openings in said passivation layer, and wherein said overlying metal layer comprises nickel;

depositing an adhesive material on a substrate;

after said depositing said adhesive material, joining said die and said substrate using said adhesive material, wherein an opening in said substrate exposes said overlying metal layer; and

after said joining said die and said substrate, forming a metal conductor through said opening in said substrate.

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Reconsiderations of Claims 197 and 202 rejected under 35 U.S.C. 102(e) as being anticipated by Fillion et al. (U.S. Pat. No. 6,306,680) are requested in accordance with the following remarks.

Applicants respectfully assert that the method currently claimed in Claim 197 patentably distinguishes over the citation by Fillion et al. (U.S. Pat. No. 6,306,680) because Fillion et al. fail to teach, hint or suggest an opening in a substrate joined with a die may exposes an overlying metal layer on multiple pads exposed by multiple opening in a passivation layer, as currently claimed in Claim 197.

Furthermore, Fillion et al. fail to teach, hint or suggest that said overlying metal layer comprises nickel, as currently claimed in Claim 197.

Furthermore, Fillion et al. fail to teach, hint or suggest that a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation

layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, wherein said overlying metal layer is on said multiple pads exposed by said multiple openings in said passivation layer, as taught on pages 9-10 of the Specification and as currently claimed in Claim 197.

Withdrawal of rejection under 35 U.S.C. 102(e) to currently-amended Claim 197 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 197 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 198-200 and 202 patently define over the prior art as well.

Conclusion

All of the pending claims are believed to be in condition for Allowance, and that is so requested.

It is requested that should Examiner Vu not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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